CLAIMS

What is claimed is:

1. A circuit structure for an analog circuit stage, comprising:
   a parallel plate capacitor formed on surface features such that said capacitor is not planar.

2. The circuit structure of Claim 1, wherein said capacitor has a dielectric layer between two conducting layers, said dielectric layer being SiO_2.

3. The circuit structure of Claim 1, wherein said capacitor has a dielectric layer between two conducting layers, at least one of said conducting layers being polysilicon.

4. The circuit structure of Claim 1, wherein said capacitor has a dielectric layer between two conducting layers, said dielectric layer being PZT.

5. The circuit structure of Claim 1, wherein said features are formed by patterning and etching the surface, and wherein said features are formed simultaneously with the placement of alignment marks.

6. A circuit structure for an analog circuit stage, comprising:
a first conducting layer;
an insulating layer formed on said first conducting layer;
a second conducting layer formed on said insulating layer to thereby form a capacitor structure;
wherein said capacitor structure is formed on surface features such that said capacitor is not planar.

7. The circuit structure of Claim 6, wherein said insulating layer is made of SiO_2.

8. The circuit structure of Claim 6, wherein said first and said second conducting layers are made from polysilicon.

9. The circuit structure of Claim 6, wherein said features are formed by patterning and etching the surface.

10. The circuit structure of Claim 6, wherein said features are formed during placement of alignment marks.

11. A semiconductor fabrication method, comprising the steps of:
forming surface features simultaneously with the formation of alignment marks on a wafer;
forming a first conducting layer over said surface features;
forming an insulating layer on said first conducting layer;
forming a second conducting layer on said insulating layer to thereby form a capacitor structure;
wherein said capacitor structure is not planar.

12. The circuit structure of Claim 11, wherein said insulating layer is SiO_2.

13. The circuit structure of Claim 11, wherein said first and said second conducting layers are polysilicon.

14. The circuit structure of Claim 11, wherein said features are formed by patterning and etching.

15. A semiconductor fabrication method, comprising the steps of:
forming a sacrificial layer of oxide on selected areas of a substrate;
stripping said sacrificial layer to form recesses in said substrate;
forming a first insulating layer on said substrate over said recesses;
forming a first conducting layer on said first insulating layer;
forming a second insulating layer on said first conducting layer;
forming a second conducting layer on said second insulating layer to thereby form a capacitor structure;
wherein said capacitor structure has non-planar surface features.

16. The circuit structure of Claim 15, wherein said second insulating layer is SiO_2.

17. The circuit structure of Claim 15, wherein said first and second conducting layers are polysilicon.